ABSTRACT

A memory device includes memory cells, bit lines, active area lines running generally in parallel to the bit lines, and transistors formed in each active area line and electrically coupling memory cells to corresponding bit lines. Each bit line includes slanted portions that intersect a corresponding portion of an active area line at an angle. Contacts electrically coupling the bit line to portions of the active area line are formed in a region generally defined by the angled intersection of the bit line to the active area line. The memory cells can have an area of about $6F^2$, and the bit lines can be coupled to sense amplifiers in a folded bit line configuration. Each bit line includes a first level portion and a second level portion.